Claims:

1. An integrated circuit comprising: a gate array architecture;

said gate array architecture including a semiconductor substrate having a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites to form N-type and P-type transistors;

wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors.

2. The integrated circuit of claim 1, wherein the ratio between the two distinct transistor sizes is on the order of one-third.

3. The integrated circuit of claim 2, wherein the ratio between the capacitance of the larger and smaller relatively sized transistors is on the order of one-third.

4. The integrated circuit of claim 1, wherein said partially overlying polysilicon landings for the smaller and larger transistors are not connected.

5. The integrated circuit of claim 4, and further comprising an interconnect overlying said gate array architecture;

the interconnect being adapted to connect the transistors of the gate array architecture to form a flip-flop.

6. The integrated circuit of claim 5, wherein the interconnect is further adapted to connect the transistors of the gate array architecture so that the internal clock buffers of the flip-flop are formed from the smaller transistors.

7. The integrated circuit of claim 6, wherein said gate array architecture is repeated in said integrated circuit.

8. The integrated circuit of claim 6, wherein said integrated circuit is incorporated in a communications device.

9. The integrated circuit of claim 6, wherein said integrated circuit is attached to a motherboard.

10. The integrated circuit of claim 9, wherein said integrated circuit is in incorporated in a personal computer.

11. The integrated circuit of claim 10, wherein said personal computer comprises one of a laptop and a desktop computer.

12. The integrated circuit of claim 1, wherein successive rows of small diffusion regions are followed by successive rows of regular-sized diffusion regions;

wherein immediately successive rows within similarly-sized diffusion regions have opposite polarity.

13. A method of fabricating an integrated circuit chip comprising:

processing a semiconductor substrate to form a gate array architecture of transistors in the substrate, the gate array architecture comprising a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites to form N-type and P-type transistors;

wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors.

14. The method of claim 13, wherein said semiconductor substrate comprises a silicon substrate.

15. The method of claim 14, wherein processing said silicon substrate to form a gate array architecture comprises:

forming said partially overlying polysilicon landings so that said landings for the smaller and larger transistors are not connected.

16. The method of claim 15, wherein the ratio between the two distinct transistor sizes is on the order of one-third.

17. The method of claim 16, wherein the ratio between the capacitance of the larger and smaller relatively sized transistors is on the order of one-third.

18. The method of claim 15, and further comprising:

forming a metallization interconnect overlying said gate array architecture.

19. The method of claim 18, wherein forming a metallization interconnect comprises forming a metallization interconnect that connects the transistors of the gate array architecture to form a flip-flop.

20. The method of claim 19, wherein forming a metallization interconnect comprises forming an interconnect that connects the transistors of the gate array architecture so that the internal clock buffers of the flip-flop are formed from the smaller transistors.

21. An article comprising: a storage medium, said storage medium having instructions stored thereon, said instructions, when executed, resulting in the capability to design the layout of an integrated circuit chip for fabrication, the integrated circuit chip including a gate array architecture, the gate array architecture comprising a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites to form N-type and P-type transistors;

wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors.

22. The article of claim 21, wherein said instructions, when executed, result in the capability to design the layout of the gate array architecture, wherein the ratio between the two distinct transistor sizes is on the order of one-third.

23. The article of claim 22, wherein said instructions, when executed, result in the capability to design the layout of the gate array architecture, wherein said partially overlying polysilicon landings for the smaller and larger transistors are not connected.

24. The article of claim 23, wherein said instructions, when executed, result in the capability to design the layout of a metallization interconnect overlying said gate array architecture.

25. The article of claim 24, wherein said instructions, when executed, result in the capability to design the layout of a metallization interconnect overlying said gate array architecture, wherein said metallization interconnect couples the transistors of the gate array architecture to form a flip-flop.

26. The article of claim 25, wherein said instructions, when executed, result in the capability to design the layout of a metallization interconnect overlying said gate array architecture that connects the transistors of the gate array architecture so that the internal clock buffers of the flip-flop are formed from the smaller transistors.